

Abstract:

Method and Integrated Circuit for Increasing the Immunity to Interference

The invention describes a method of improving the immunity to interference of an integrated circuit (16), wherein error signals are transferred between at least one microprocessor chip or multiple processor μ C (1) and at least one additional component (2) in the form of one or more error signals, and for the transfer, a minimum pulse length that is independent of the clock frequency of the microprocessor or the microprocessors is defined, starting from which a signal on an error line having a defined pulse length is interpreted as an error.

The invention also relates to an integrated circuit, which is designed in particular in such a fashion that the above method is implemented, comprising

- at least one microprocessor chip or multiple processor microcontroller (1) or microprocessor module and at least one additional component (2) comprising in particular separately arranged power elements, and
- one or more pulse extending devices and/or signal delaying devices for the output of error pulses (6, 6') one after the other through at least one error line (3, 4).

(Figure 1)